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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,811	STEFAN ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-83 is/are pending in the application.
- 4a) Of the above claim(s) 1-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22-25, 28, 30-34, 38, 43, 44, 47, 51, 52, 59, 78 and 83 is/are rejected.
- 7) ☒ Claim(s) 26, 27, 29, 35-37, 39-42, 45, 46, 48-50, 53-58 and 60-77 is/are objected to.
- 8) ☒ Claim(s) 1-21 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 22-83 have been examined.
2. It is hereby acknowledged that the following papers have been received and placed of record in the file: amendment filed 03/02/2007.

Claim Objections

3. Applicant, via amendment, has overcome the objections to claims 33 and 34 set forth in the previous Office Action. Consequently, these objections are withdrawn by the examiner.

4. Claims 22, 82, and 83 are objected to because of the following informalities:

Regarding claims 22 and 83, the limitation "said clock device outputting and synchronizing clock signal to said associative device and said controller" should be changed to "said clock device outputting said synchronizing clock signal to said associative device and said controller".

Regarding claim 82, the limitation "a memory device" at line 2 should be changed "an associative memory device" to make language consistent with the rest of the claim.

Claim Rejections - 35 USC § 112

5. Applicant, via amendment, has overcome the 35 U.S.C. § 112, second paragraph, rejections set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 22-25, 28, 30-34, 38, 43, 44, 47, 51, 52, 59, and 78-83 are rejected under 35 U.S.C. 102(e) as being anticipated by Stefan et al., U.S. Patent No. 6,760,821 (Hereinafter Stefan).

8. Referring to claim 22, Stefan has taught a data processing system, said data processing system comprising:

an associative memory device [*connex memory; Fig. 2, component 206*]
containing n-cells [*column 4, lines 20-41*], each of said n-cells including a processing circuit [*comparator; Fig. 14, component 55*] and m-bits of memory capacity [*column 17, lines 10-15, 45-49*];

a controller [Fig. 1, component 255] for issuing one of a plurality of instructions to said associative memory device [column 4, lines 10-19], the plurality of instructions comprising a "right limit" command ["set-limit" command; column 11, lines 1-6];

a clock device [Fig. 1, component 256] for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said clock device outputting said synchronizing clock signal to said associative memory device and said controller [column 4, lines 7-14]; and

wherein said controller globally communicates one of said plurality of instructions to all of said n-cells simultaneously, within one of said clock cycles [column 5, lines 31-49].

9. Referring to claim 23, Stefan has taught the data processing system of claim 22, further comprising:

a classification device [transcoders; Fig. 12, components 39 & 40] for selectively operating in association with a local state [marked state] of each of said n-cells [column 18, lines 28-35, 45-50]; and

wherein one of said plurality of instructions is executed by selected cells within said associative memory device in dependence upon said local state of said n-cells as directed by said classification device [column 16, lines 44-60], said execution of said instruction occurring simultaneously in each of said selected cells within one of said clock cycles [column 5, lines 31-36].

10. Referring to claim 24, Stefan has taught the data processing system of claim 23, wherein: each of said n-cells include a state field [marker field] and a data field [symbol

field], said state field comprising a marker bit for encoding a local state of each of said n-cells, thereby indicating one of a marked state and a non-marked state of each of said n-cells [column 3, lines 60-67; column 17, lines 10-15].

11. Referring to claim 25, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a 'load line immediate' command [*"write-all"*] whereby the contents of all of said n-cells in said marked state are replaced with data indicated by said 'load line immediate' command [column 8, lines 53-58].

12. Referring to claim 28, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a 'left limit' command [*"set-limit"*] whereby a left limit of a search space is set to a leftmost cell of said n-cells in said marked state [column 11, lines 1-6].

13. Referring to claim 30, Stefan has taught the data processing system of claim 24, wherein: said controller may dynamically limit a search space within said n-cells [column 10, lines 54-67].

14. Referring to claim 31, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a 'find' command whereby each of said n-cells holding values equal to an argument indicated by said 'find' command is identified; and wherein said 'find' command sets said marker bit to said marked state in each of said n-cells located to the right of said identified n-cells, and sets said marker bit to said non-marked state in all other of said n-cells [column 6, lines 36-64].

15. Referring to claim 32, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `match` command [*"c-find"*] whereby each of said n-cells having a marker bit in said marked state and having said data field matching an argument indicated by said `match` command [*"c-find"*], is identified; and wherein said `match` command sets said marker bit to said marked state in each of said n-cells following said identified n-cells, and sets said marker bit to said non-marked state in all other of said n-cells [*column 6, line 65 – column 7, line 22*].

16. Referring to claim 33, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `find and mark left` command [*"Reverse-find"*] whereby each of said n-cells holding values equal to an argument indicated by said `find and mark left` command is identified; and wherein said `find and mark left` command [*"Reverse-find"*] sets said marker bit to said marked state in each of said n-cells located to the left of said identified n-cells, and sets said marker bit to said non-marked state in all other of said n-cells [*column 10, lines 22-27*].

17. Referring to claim 34, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `match and mark left` command [*"Reverse-cfind"*] whereby each of said n-cells having a marker bit in said marked state and having said data field matching an argument indicated by said `match and mark left` command [*"Reverse-cfind"*], is identified; and wherein said `match and mark left` command sets said marker bit to said marked state in each of said n-cells located to the left of said identified n-cells [*column 10, lines 28-35*].

18. Referring to claim 38, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `clr` command *["jump"]* whereby said marker bit of each of said n-cells containing a value equal to an argument indicated by said `clr` command *["jump"]* is set to said non-marked state *[column 9, lines 4-14]*.

19. Referring to claim 43, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `left` command *["delete"]* whereby all of said marker bits for said n-cells are shifted leftward by one *[column 8, lines 15-25]*.

20. Referring to claim 44, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `right` command *["insert"]* whereby all of said marker bits for said n-cells are shifted rightward by one *[column 7, line 65 – column 8, line 14]*.

21. Referring to claim 47, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `nop` command *["set-limit-address"]* whereby no operation is executed *[column 11, lines 7-10]*.

22. Referring to claim 51, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `set` command *["write-one"]* whereby a value indicated by said `set` command *["write-one"]* is stored in a leftmost of said n-cells in said marked state *[column 8, lines 48-52]*.

23. Referring to claim 52, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a 'setall' command ["write-all"] whereby a value indicated by said 'setall' command ["write-all"] is stored in all of said n-cells in said marked state *[column 8, lines 53-58]*.

24. Referring to claim 59, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a 'ld' command ["write-all"] whereby a value indicated by said 'ld' command ["write-all"] is loaded into said data field in all of said n-cells in said marked state *[column 8, lines 53-58]*.

25. Referring to claim 78, Stefan has taught the data processing system of claim 22, wherein:

said classification device *[transcoders; Fig. 12, components 39 & 40]* determines a global state *[Line-in [1] state]* of each of said n-cells *[column 16, lines 44-60]*; and

wherein said one of said plurality of instructions is executed by selected cells within said associative memory device in dependence upon both said local state *[marked state]* and said global state *[Line-in [1] state]* of said n-cells *[column 16, lines 44-60]*, said execution of said instruction occurring simultaneously in each of said selected cells within one of said clock cycles *[column 5, lines 31-36]*.

26. Referring to claim 79, Stefan has taught the data processing system of claim 22, wherein: said associative memory device allows the use of variable-length key fields *[the connex memory allows the use of variable-length character strings (i.e. key fields); column 4, lines 20-30]*.

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27. Referring to claim 80, Stefan has taught the data processing system of claim 79, wherein:

said variable-length key fields include a data field and an attached key field, each of said n-cells having said data field and said key field [*column 4, lines 20-30*]; and

wherein data stored in each of said n-cells is alternatively considered as part of said data field and said attached key field at different times during execution of one of said plurality of instructions [*column 4, lines 20-30*].

28. Referring to claim 81, Stefan has taught a method of processing data, said method comprising the steps of:

forming an associative memory device [*connex memory; Fig. 2, component 206*] to contain n-cells [*column 4, lines 20-41*];

configuring each of said n-cells to include a processing circuit [*Fig. 14, components 55, 61, and 62*], the processing circuit performs a plurality of operations [*the comparator and mux circuits perform select operations and compare operations; column 17, lines 10-49*];

issuing one of a plurality of instructions from a controller [*Fig. 1, component 255*] to said associative memory device [*column 4, lines 10-19*];

utilizing a clock device [*Fig. 1, component 256*] for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said clock device outputting said synchronizing clock signal to said associative memory device and said controller [*column 4, lines 7-14*]; and

globally communicating one of said plurality of instructions from said controller to all of said n-cells simultaneously, within one of said clock cycles *[column 5, lines 31-49]*.

29. Referring to claim 82, Stefan has taught a data processing system, said data processing system comprising:

a memory device *[connex memory; Fig. 2, component 206]* containing n-cells *[column 4, lines 20-41]*, each of said n-cells including a processing circuit *[Fig. 14, components 55, 61, and 62]*, the processing circuit performs a plurality of operations *[the comparator and mux circuits perform select operations and compare operations; column 17, lines 10-49]*;

a controller *[Fig. 1, component 255]* for issuing one of a plurality of instructions to said associative memory device *[column 4, lines 10-19]*;

a clock device *[Fig. 1, component 256]* for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said clock device outputting said synchronizing clock signal to said associative memory device and said controller *[column 4, lines 7-14]*; and

wherein said controller globally communicates one of said plurality of instructions to all of said n-cells simultaneously, within one of said clock cycles *[column 5, lines 31-49]*.

30. Referring to claim 83, Stefan has taught a data processing system, said data processing system comprising:

an associative memory device *[connex memory; Fig. 2, component 206]* containing n-cells *[column 4, lines 20-41]*, each of said n-cells including a processing

circuit [Fig. 14, components 55, 61, and 62], the processing circuit performs a plurality of computations [the comparator and mux circuits perform select computations and compare computations; column 17, lines 10-49];

a controller [Fig. 1, component 255] for issuing one of a plurality of instructions to said associative memory device [column 4, lines 10-19];

a clock device [Fig. 1, component 256] for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said clock device outputting and synchronizing clock signal to said associative memory device and said controller [column 4, lines 7-14]; and

wherein said controller globally communicates one of said plurality of instructions to all of said n-cells simultaneously, within one of said clock cycles [column 5, lines 31-49].

Response to Arguments

31. Applicant's arguments filed 03/02/2007 have been fully considered but they are not persuasive.

32. Applicant argues the novelty/rejection of claims 22-80 on pages 22-23 of the remarks, in substance that:

"On page 11 of the Office Action, it is asserted that the data indicated by the 'right limit' command 'ha[s]' not been found in the prior art and would not have been obvious as the instructions are unique to the architecture of Applicant's data processing system.' Since Claims 23-25, 28, 30-34, 38, 43, 44, 47, 51, 52, 59, and 78-80 are dependent upon base Claim 22, Applicant's submit that Stefan does not anticipate Claims 23-25, 28, 30-34, 38, 43, 44, 47, 51, 52, 59, and 78-80." (page 23)

These arguments are not found persuasive for the following reasons:

In the non-final office action mailed 10/31/2006 (Hereinafter NFOA), the examiner indicated that claim 29, which claims a "right limit" command, "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims" (See NFOA paragraph 32). However, the applicant has not written claim 29 in independent form. The amendment to claim 22 (the base claim for claims 23-25, 28, 30-34, 38, 43, 44, 47, 51, 52, 59, and 78-80) indicates that one of the plurality of instructions is a "right limit" command. However, since the description of the "right limit" command included in claim 29 is not included in claim 22, claim 22 is not allowable for the reasons given in the NFOA.

33. Applicant's arguments with respect to claim 81-83 have been considered but are moot in view of the new ground(s) of rejection (a different interpretation of Stefan), which was necessitated by amendment.

Allowable Subject Matter

34. As noted in the non-final office action mailed 10/31/2006, claims 26, 27, 29, 35-37, 39-42, 45, 46, 48-50, 53-58, and 60-77 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. A statement of reasons for indication of allowable subject matter was given in the non-final office action mailed 10/31/2006 and is copied below for the applicant's convenience.

36. The following is a statement of reasons for the indication of allowable subject matter: Claims 26, 27, 29, 35-37, 39-42, 45, 46, 48-50, 53-58, and 60-77 are directed towards particular instructions issued by the claimed data processing system. The instructions as claimed have not been found in the prior art and would not have been obvious as the instructions are unique to the architecture of Applicant's data processing system.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181

A handwritten signature in black ink, appearing to read "Donald Sparks", is written over a circular stamp.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER